EKF SYSTEM

User Guide

CC5-RAVE • *CompactPCI®* FC-PGA 370 CPU

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Contents

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About this Manual

This manual describes the technical aspects of the CC5-RAVE, required for installation and system integration. It is intended for the experienced user only.

Edition History

Document	Ed.	Contents/*Changes*	Author	Date
Text # 2331 cc5uge.wpd	1	1. Edition User Manual CC5-RAVE English Initial edition, to be completed later on	jj	27. June 2000
	2	Preliminary edition (PanelLink logo included)	jj	15. Aug 2000
	3	Preliminary edition (photographic images included)	jj	15. Sep 2000
	4	Manual reflects board revision Rev.1 now, added CC5-RAVE special features (watchdog, programmable LED, PXI trigger signals, hot swap detection), new processor speeds	gn/jj	25. Jan 2001
	5	Added sections “Local PCI Devices” and “Local SMB Devices” to chapter “Technical Reference”.	gn	09. Apr 2001
	6	Manual reflects board revision Rev.2: Changed CC6-ACID block diagram and images, changed illustration 'Component Assembly', Low Pin Count Interface connector PLPC either top or bottom use, modified tables 'Processors Currently Supported', added chapter 'Thermal Considerations' and tables 'Power Consumption' and 'Throttle Mode vs. Temperature', changed front panel illustration, modified LED descriptions	jj	3 May 2002
	7	Added images CC6-ACID top/bottom attachment (chapter 'LPC Interface')	jj	23 May 2002

Related Documents

For a description of the CC5-RAVE BIOS see document 'CC5-RAVE BIOS Quick Reference', available by download at http://www.ekf.de/c/ccpu/cc5/cc5.html.

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

Pentium, Celeron, Socket 370: ® Intel
CompactPCI : ® PICMG
Windows 98, Windows NT, Windows 2000: ® Microsoft

EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

CC5-RAVE Features

Feature Summary CC5-RAVE	
Form Factor	Single size *CompactPCI* style Eurocard (160x100mm^2), front panel width 4HP (20.3mm)
Processor	Support for Intel® Celeron™, Pentium®-III and *VIA Cyrix® III* processor, 370-pin PPGA or FC-PGA package
Chipset	i810E chipset consisting of: • 82810E Graphics/memory Controller Hub (GMCH) • 82801 I/O Controller Hub (ICH0) • 82802 Firmware Hub (FWH)
Memory	• 144-pin dual inline memory module (SO-DIMM) socket, module height 1.05inch (26.7mm) max. • Support for up to 256MB, non ECC, unbuffered synchronous DRAM (SDRAM) • Support for serial presence detect (SPD) and non-SPD SO-DIMMs , PC-100 style
Video I/O	Analog monitor and digital flat-panel display support by DVI-I connector (front panel), up to 1280x1024 pixel 16M colors 85Hz refresh rate, incorporates PanelLink Digital technology (Silicon Image)
USB I/O	Single type A connector (front panel), USB1.1, data transfer rate of up to 12Mbit/s
Ethernet I/O	100Base-Tx/10Base-T Fast-Ethernet controller, 82559ER chip, RJ-45 connector (front panel), 100Mbps full-duplex, auto-negotiation
Legacy I/O	LPC Super-I/O interface connector, CC6-ACID companion board with Super-I/O controller available
IDE/ATA	• Ultra ATA/66 40-pin connector (primary IDE port) • CompactFlash socket for CFA ATA cards utilizing 'True IDE Mode' (secondary IDE port)
CompactPCI	32-bit, 33.3MHz, PCI bridge chip Texas Instruments PCI2050, 133MBps CPCI master
BIOS	General Software Embedded 2000 BIOS, 2..8Mbit flash memory (82802AA, 82802AB, 82802AC firmware hub)

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Short Description

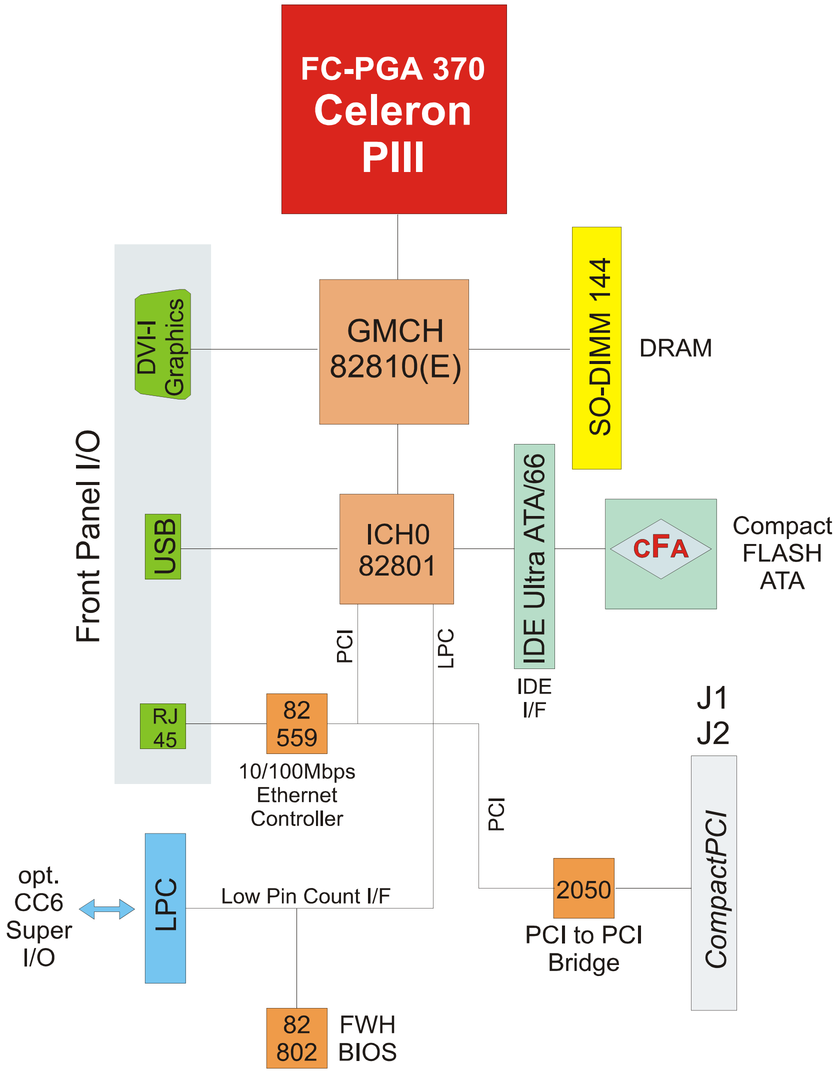
Likewise equipped with the Intel Celeron® or Pentium-III® processor, the CC5-RAVE is a powerful 3U (single size Eurocard) CPU board, well suitable for any CompactPCI® systems.

The board is provided with the chip set 810(E), which contains an embedded graphics controller. The DVI-I interface allows for attachment of both, advanced and legacy flat panel displays and CRT monitors. The on-board USB-port is an universal interface to a variety of peripheral devices, as keyboard, mouse, printer, modem, or video camera. For high speed networking, the CC5-RAVE is provided with a 10/100Mbps Fast Ethernet twisted pair jack. All connectors mentioned above are comfortably available from the cards front panel.

As a mass storage interface, the CC5-RAVE provides for an Ultra ATA/66 connector, suitable for any EIDE harddisk and CD-ROM. A receptacle for CompactFlash cards allows utilization of silicon disks. The main memory is a SO-DIMM 144 form factor module up to 256MB. The jumperless board can be used with a front-side bus clock of up to 100(133)MHz.

Equipped with a PCI-bridge chip, the CC5-RAVE offers a full CPCI interface for reliable system expansion. Especially designed for embedded systems applications, the *General Software* BIOS is maintained by EKF. So custom specific enhancements can be realized at anytime.

Block Diagram



Block Diagram
CC5-RAVE

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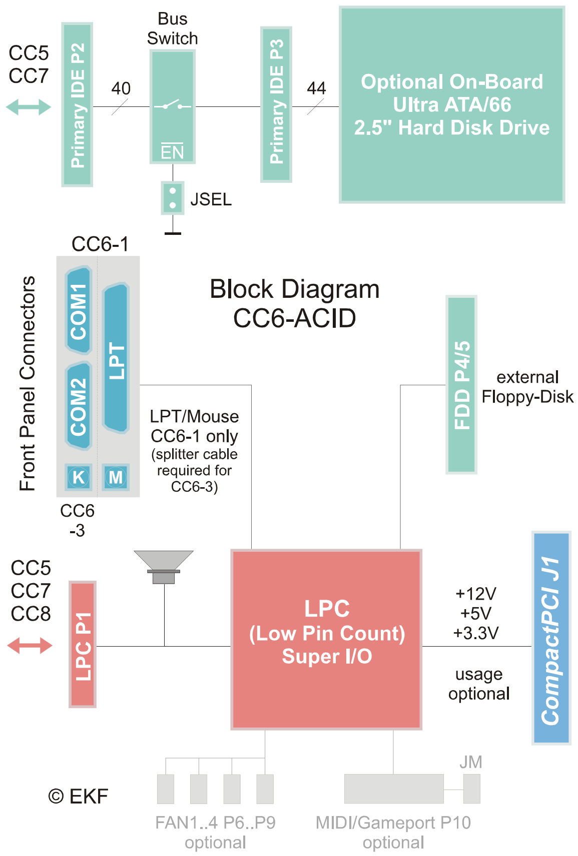
Expansion Module CC6-ACID

Available as a companion board to the CC5-RAVE, the CC6-ACID is provided with all PC legacy I/O ports. This module fits on either side of the CC5, top (CC6-1 and CC6-3) or bottom (CC6-3 only), utilizing the LPC Low Pin Count interface. The card will be required only if the classical interfaces, e.g. serial and parallel port remain in use in a given application.

The CC6-ACID can be delivered with an on-board 2.5" hard disk, resulting in a very compact system. The connectors LPT (CC6-1 only), COM1/2, mouse and keyboard are situated at the front panel, while a floppy disk drive can be attached via the on-board pin header. While the CC6-1 requires 8HP, the CC6-3 is equipped with a 4HP front panel.



CC5-RAVE & CC6-ACID

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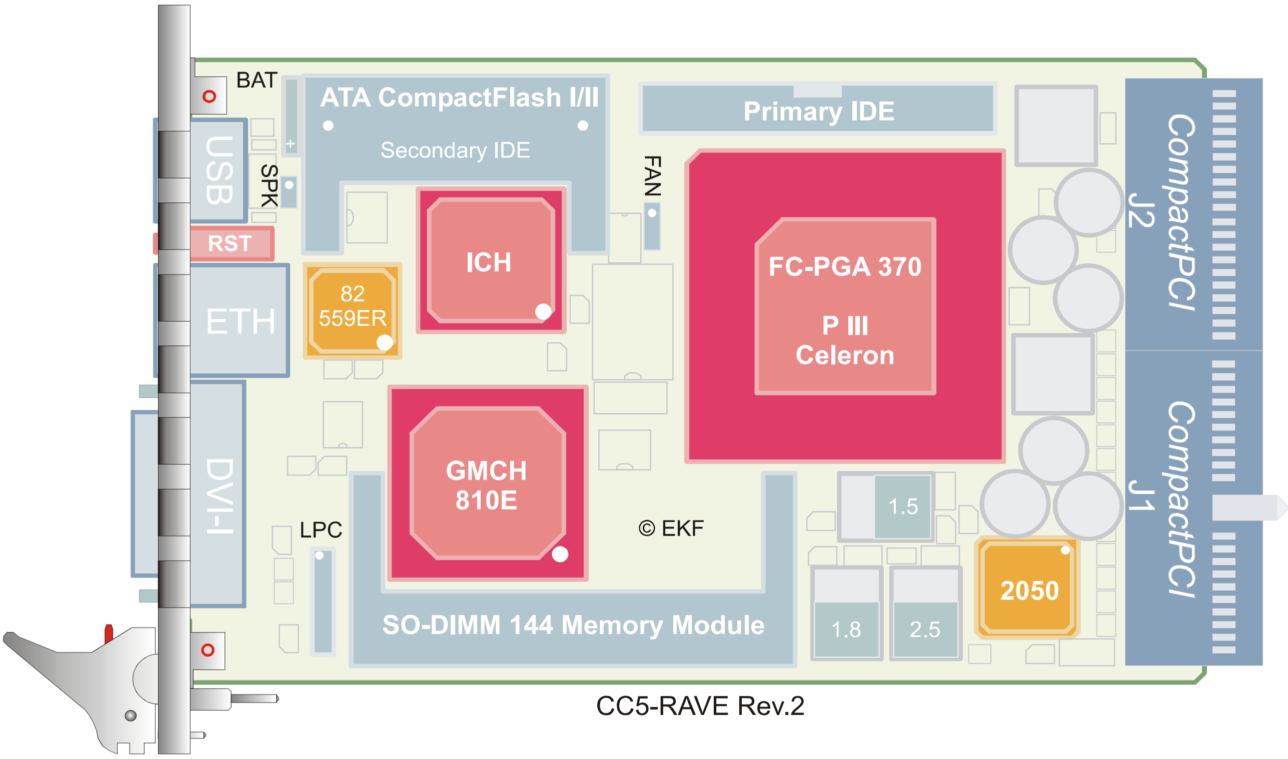
Top View Component Assembly



Strapping Headers

ISPCON	In System Programmable GAL (PLD programming), not stuffed
JFAN	Cooling fan connector, 12V or 5V fixed operation
JSPKR	Speaker connector

Connectors & Sockets

CFA1	CompactFlash ATA socket (secondary EIDE interface)
J1/J2	*CompactPCI* Bus
PLPCT PLPCB	Low Pin Count expansion interface connector (Super-I/O), available either from top (T) or bottom (B) of the board
PIDE	Ultra ATA/66 connector (primary IDE interface)
PITP	CPU Debug Port, not stuffed
SODIMM1	144-pin memory module

Front Panel Elements

Ethernet	100BaseTX/10BaseT, RJ-45 receptacle with indicator LEDs
Graphics	DVI-I receptacle, suitable for DVI digital flat panel displays and/or analog monitors
USB	Universal Serial Bus 1.1 self powered root hub, type A receptacle
Reset	Push-button switch with indicator LED (power good)
IDE	LED indicating IDE activity

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Microprocessor

The CC5-RAVE supports 370-pin PPGA and FC-PGA socketed Celeron processors and FC-PGA housed Pentium-III processors listed below. The FC-PGA processors are also known as Coppermine 0.18u generation (CPU ID 068xh). The CC5 is not suitable for newly available Tualatin 0.13u FC-PGA2 processors. The CC5 is also not suitable for older slot style Celeron and Pentium-II processors. The Socket 370 also is not compatible with Socket 7 processors (e.g. Pentium-MMX, K6). The table below lists typical processors available for the CC5-RAVE (there might be other ressources not mentioned here). Please note: Use of any processor not supported can cause permanent damage to the processor and the CC5-RAVE!

Neither have all of the CPU types mentioned in the tables below been tested by EKF for use with the CC5-RAVE, nor does EKF claim that the entire range of processors is available for purchase. Instead, please refer to the EKF price list http://www.ekf.de/liste/liste_20.html for availability of the CC5-RAVE with particular processors (your individual request to sales@ekf.de is very welcome).

Please do not attempt to change or remove the installed processor by yourself. The CC5-RAVE is equipped with a non-ZIF processor socket, which requires special handling to remove the CPU. In addition, the passive heatsink is fixed by several screws, which need to be precisely adjusted in order achieve the optimum heat conduction. Furthermore, the heatsink is fixed with conductive pads and/or adhesion to the Coppermine processors hot spot, which cannot be removed and renewed without suitable material and knowledge. If it is required to identify a particular processor, use suitable software instead, like Intels freely available Processor Frequency ID Utility.

Do not confuse the processor host bus frequency (FSB front side bus) with the memory speed or the PCI clock, which are independent from each other. The processor signals its appropriate basic speed by two pins to the chipset, which is thereby adjusted automatically (no user interaction required). The internal CPU speed is achieved by multiplying the host bus frequency by a fixed value.

The CC5-RAVE is powered across the CompactPCI connectors J1/J2 (3.3V, 5V, 12V). The processor core voltage is generated by a switched voltage regulator, sourced from the 5V plane. Any FC-PGA 370 processor signals its required core voltage by 4 (Intel) dedicated pins, hence there is no need (no choice) for user adjustment. Manipulation of these parameters (the euphemistic term 'tuning' is widely in use for that) may lead to unpredictable results.

Celeron® Processors Currently Supported (as of 05/2002)						
Processor	Speed	Host Bus	L2 Cache	CPU ID	Package	Stepping
Celeron 1.1G	1.1GHz	100MHz	128KB	068Ah	FC-PGA	D0
Celeron 1G	1GHz	100MHz	128KB	068Ah	FC-PGA	D0
Celeron 950	950MHz	100MHz	128KB	068Ah	FC-PGA	D0
Celeron 900	900MHz	100MHz	128KB	068Ah	FC-PGA	D0
Celeron 850	850MHz	100MHz	128KB	068Ah	FC-PGA	D0
Celeron 850	850MHz	100MHz	128KB	0686h	FC-PGA	C0
Celeron 800	800MHz	100MHz	128KB	068Ah	FC-PGA	D0
Celeron 800	800MHz	100MHz	128KB	0686h	FC-PGA	C0
Celeron 766	766MHz	66MHz	128KB	068Ah	FC-PGA	D0
Celeron 766	766MHz	66MHz	128KB	0686h	FC-PGA	C0
Celeron 733	733MHz	66MHz	128KB	068Ah	FC-PGA	D0
Celeron 733	733MHz	66MHz	128KB	0686h	FC-PGA	C0
Celeron 700	700MHz	66MHz	128KB	0686h	FC-PGA	C0
Celeron 700	700MHz	66MHz	128KB	0683h	FC-PGA	B0
Celeron 667	667MHz	66MHz	128KB	0686h	FC-PGA	C0
Celeron 667	667MHz	66MHz	128KB	0683h	FC-PGA	B0
Celeron 633	633MHz	66MHz	128KB	0686h	FC-PGA	C0
Celeron 633	633MHz	66MHz	128KB	0683h	FC-PGA	B0
Celeron 600	600MHz	66MHz	128KB	0686h	FC-PGA	C0
Celeron 600	600MHz	66MHz	128KB	0683h	FC-PGA	B0
Celeron 566	566MHz	66MHz	128KB	068Ah	FC-PGA	D0
Celeron 566	566MHz	66MHz	128KB	0686h	FC-PGA	C0
Celeron 566	566MHz	66MHz	128KB	0683h	FC-PGA	B0
Celeron 533A	533MHz	66MHz	128KB	0683h	FC-PGA	B0
Celeron 533	533MHz	66MHz	128KB	0665h	PPGA	B0
Celeron 500	500MHz	66MHz	128KB	0665h	PPGA	B0
Celeron 466	466MHz	66MHz	128KB	0665h	PPGA	B0
Celeron 433	433MHz	66MHz	128KB	0665h	PPGA	B0
Celeron 400	400MHz	66MHz	128KB	0665h	PPGA	B0
Celeron 366	366MHz	66MHz	128KB	0665h	PPGA	B0
Celeron 333	333MHz	66MHz	128KB	0665h	PPGA	B0
Celeron 300A	300MHz	66MHz	128KB	0665h	PPGA	B0

Pentium-III® Processors Currently Supported (as of 05/2002)						
Processor	Speed	Host Bus	L2 Cache	CPU ID	Package	Stepping
Pentium-III 1.13G	1.13GHz	133MHz [1]	256KB	068Ah	FC-PGA	D0
Pentium-III 1.1G	1.1GHz	100MHz	256KB	068Ah	FC-PGA	D0
Pentium-III 1BG	1GHz	133MHz [1]	256KB	068Ah	FC-PGA	D0
Pentium-III 1BG	1GHz	133MHz [1]	256KB	0686h	FC-PGA	C0
Pentium-III 1G	1GHz	100MHz	256KB	068Ah	FC-PGA	D0
Pentium-III 933	933MHz	133MHz [1]	256KB	068Ah	FC-PGA	D0
Pentium-III 933	933MHz	133MHz [1]	256KB	0686h	FC-PGA	C0
Pentium-III 933	933MHz	133MHz [1]	256KB	0683h	FC-PGA	B0
Pentium-III 900	900MHz	100MHz	256KB	068Ah	FC-PGA	D0
Pentium-III 900	900MHz	100MHz	256KB	0686h	FC-PGA	C0
Pentium-III 866	866MHz	133MHz [1]	256KB	068Ah	FC-PGA	D0
Pentium-III 866	866MHz	133MHz [1]	256KB	0686h	FC-PGA	C0
Pentium-III 866	866MHz	133MHz [1]	256KB	0683h	FC-PGA	B0
Pentium-III 850	850MHz	100MHz	256KB	068Ah	FC-PGA	D0
Pentium-III 850	850MHz	100MHz	256KB	0686h	FC-PGA	C0
Pentium-III 850	850MHz	100MHz	256KB	0683h	FC-PGA	B0
Pentium-III 800EB	800MHz	133MHz [1]	256KB	068Ah	FC-PGA	D0
Pentium-III 800EB	800MHz	133MHz [1]	256KB	0686h	FC-PGA	C0
Pentium-III 800EB	800MHz	133MHz [1]	256KB	0683h	FC-PGA	B0
Pentium-III 800EB	800MHz	133MHz [1]	256KB	0681h	FC-PGA	A2
Pentium-III 800	800MHz	100MHz	256KB	068Ah	FC-PGA	D0
Pentium-III 800	800MHz	100MHz	256KB	0686h	FC-PGA	C0
Pentium-III 800	800MHz	100MHz	256KB	0683h	FC-PGA	B0
Pentium-III 800	800MHz	100MHz	256KB	0681h	FC-PGA	A2
Pentium-III 750	750MHz	100MHz	256KB	068Ah	FC-PGA	D0
Pentium-III 750	750MHz	100MHz	256KB	0686h	FC-PGA	C0
Pentium-III 750	750MHz	100MHz	256KB	0683h	FC-PGA	B0
Pentium-III 750	750MHz	100MHz	256KB	0681h	FC-PGA	A2
Pentium-III 733	733MHz	133MHz [1]	256KB	068Ah	FC-PGA	D0
Pentium-III 733	733MHz	133MHz [1]	256KB	0686h	FC-PGA	C0
Pentium-III 733	733MHz	133MHz [1]	256KB	0683h	FC-PGA	B0
Pentium-III 733	733MHz	133MHz [1]	256KB	0681h	FC-PGA	A2

Pentium-III® Processors Currently Supported (as of 05/2002)						
Processor	Speed	Host Bus	L2 Cache	CPU ID	Package	Stepping
Pentium-III 700	700MHz	100MHz	256KB	068Ah	FC-PGA	D0
Pentium-III 700	700MHz	100MHz	256KB	0686h	FC-PGA	C0
Pentium-III 700	700MHz	100MHz	256KB	0683h	FC-PGA	B0
Pentium-III 700	700MHz	100MHz	256KB	0681h	FC-PGA	A2
Pentium-III 667	667MHz	133MHz [1]	256KB	0686h	FC-PGA	C0
Pentium-III 667	667MHz	133MHz [1]	256KB	0683h	FC-PGA	B0
Pentium-III 667	667MHz	133MHz [1]	256KB	0681h	FC-PGA	A2
Pentium-III 650	650MHz	100MHz	256KB	0686h	FC-PGA	C0
Pentium-III 650	650MHz	100MHz	256KB	0683h	FC-PGA	B0
Pentium-III 650	650MHz	100MHz	256KB	0681h	FC-PGA	A2
Pentium-III 600EB	600MHz	133MHz [1]	256KB	0686h	FC-PGA	C0
Pentium-III 600EB	600MHz	133MHz [1]	256KB	0683h	FC-PGA	B0
Pentium-III 600EB	600MHz	133MHz [1]	256KB	0681h	FC-PGA	A2
Pentium-III 600E	600MHz	100MHz	256KB	0686h	FC-PGA	C0
Pentium-III 600E	600MHz	100MHz	256KB	0683h	FC-PGA	B0
Pentium-III 600E	600MHz	100MHz	256KB	0681h	FC-PGA	A2
Pentium-III 550E	550MHz	100MHz	256KB	0683h	FC-PGA	B0
Pentium-III 550E	550MHz	100MHz	256KB	0681h	FC-PGA	A2
Pentium-III 533EB	533MHz	133MHz [1]	256KB	0683h	FC-PGA	B0
Pentium-III 533EB	533MHz	133MHz [1]	256KB	0681h	FC-PGA	A2
Pentium-III 500E	500MHz	100MHz	256KB	0683h	FC-PGA	B0
Pentium-III 500E	500MHz	100MHz	256KB	0681h	FC-PGA	A2

[1] 133MHz host bus frequency supported only with 810E chipset

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Thermal Considerations

In order to avoid malfunctioning of the CC5-RAVE, take care of appropriate cooling of the processor and system, e.g. by a cooling fan suitable to the maximum power consumption of the CPU chip actually in use. Please note, that the processors temperature is steadily measured by a special controller (MAX1617), attached to the onboard SMBus® (System Management Bus). The processor core (die) temperature is signalled by the forward voltage of a CPU integrated diode. A second diode internal to the MAX1617 allows for acquisition of the boards surface temperature. The programmable overtemperature alarm allows to trigger the SMBus alert line in order to avoid overheating. A suitable software to display both, the die temperature, as well as the board temperature, is MBM (Motherboard Monitor), which can be downloaded from the web. After installation, both temperatures can be observed permanently from the Windows taskbar.

By default, the CC5-RAVE is equipped with a passive heatsink, covering not only the processor chip itself but also major areas on the board, for an optimum thermal conduction. In addition, a forced vertical air flow trough the system enclosure (e.g. bottom mount fan unit) is strongly recommended. Be sure to thoroughly discuss your actual cooling needs with EKF. Generally, the faster the CPU speed the higher is its power consumption.

The maximum power consumption and operating temperature of a particular processor can be derived from the tables below. Fortunately, the power consumption is by far lower when executing typical Windows or Linux tasks. The heat dissipation increases especially when rendering software is executed, e.g. the Acrobat Distiller. EKF tests the CC5-RAVE by running 'kpower.exe', a proprietary Intel tool for generating the maximum stress to the processor.

Celeron® Processors Maximum Power Consumption and Die Temperature					
Processor	Speed	Host Bus	CPU ID	maximum Power	max. Die Temperature
Celeron 1.1G	1.1GHz	100MHz	068Ah	33.0W	77°C
Celeron 1G	1GHz	100MHz	068Ah	29.0W	75°C
Celeron 950	950MHz	100MHz	068Ah	28.0W	79°C
Celeron 900	900MHz	100MHz	068Ah	26.7W	77°C
Celeron 850	850MHz	100MHz	068Ah	25.7W	80°C
Celeron 850	850MHz	100MHz	0686h	22.5W	80°C
Celeron 800	800MHz	100MHz	068Ah	24.5W	80°C
Celeron 800	800MHz	100MHz	0686h	20.8W	80°C
Celeron 766	766MHz	66MHz	068Ah	23.6W	80°C
Celeron 766	766MHz	66MHz	0686h	20.0W	80°C
Celeron 733	733MHz	66MHz	068Ah	22.8W	80°C
Celeron 733	733MHz	66MHz	0686h	19.1W	80°C
Celeron 700	700MHz	66MHz	0686h	21.9W	80°C
Celeron 700	700MHz	66MHz	0683h	18.3W	80°C
Celeron 667	667MHz	66MHz	0686h	21.1W	82°C
Celeron 667	667MHz	66MHz	0683h	17.5W	82°C
Celeron 633	633MHz	66MHz	0686h	20.2W	82°C
Celeron 633	633MHz	66MHz	0683h	16.5W	82°C
Celeron 600	600MHz	66MHz	0686h	19.6W	90°C
Celeron 600	600MHz	66MHz	0683h	15.8W	90°C
Celeron 566	566MHz	66MHz	068Ah	19.2W	90°C
Celeron 566	566MHz	66MHz	0686h	14.9W	90°C
Celeron 533A	533MHz	66MHz	0683h	14.0W	90°C
Celeron 533	533MHz	66MHz	0665h	28.3W	T_case 70°C
Celeron 500	500MHz	66MHz	0665h	27.0W	T_case 70°C
Celeron 466	466MHz	66MHz	0665h	25.6W	T_case 70°C
Celeron 433	433MHz	66MHz	0665h	24.1W	T_case 85°C
Celeron 400	400MHz	66MHz	0665h	23.7W	T_case 85°C
Celeron 366	366MHz	66MHz	0665h	21.7W	T_case 85°C
Celeron 333	333MHz	66MHz	0665h	19.7W	T_case 85°C

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Pentium-III® Processors Maximum Power Consumption and Die Temperature					
Processor	Speed	Host Bus	CPU ID	maximum Power	max. Die Temperature
Pentium-III 1.13G	1.13GHz	133MHz	068Ah		
Pentium-III 1.1G	1.1GHz	100MHz	068Ah		
Pentium-III 1BG	1GHz	133MHz	068Ah	29.0W	75°
Pentium-III 1BG	1GHz	133MHz	0686h	26.1W	70°
Pentium-III 1G	1GHz	100MHz	068Ah	29.0W	75°
Pentium-III 933	933MHz	133MHz	068Ah	27.5W	77°
Pentium-III 933	933MHz	133MHz	0686h	24.5W	77°
Pentium-III 900	900MHz	100MHz	068Ah	26.7W	77°
Pentium-III 900	900MHz	100MHz	0686h	23.2W	77°
Pentium-III 866	866MHz	133MHz	068Ah	26.1W	80°
Pentium-III 866	866MHz	133MHz	0686h	22.9W	80°
Pentium-III 850	850MHz	100MHz	068Ah	25.7W	80°
Pentium-III 850	850MHz	100MHz	0686h	22.5W	80°
Pentium-III 800EB	800MHz	133MHz	068Ah	24.5W	80°
Pentium-III 800EB	800MHz	133MHz	0686h	20.8W	80°
Pentium-III 800	800MHz	100MHz	068Ah	24.5W	80°
Pentium-III 800	800MHz	100MHz	0686h	20.8W	80°
Pentium-III 750	750MHz	100MHz	068Ah	23.2W	80°
Pentium-III 750	750MHz	100MHz	0686h	19.5W	80°
Pentium-III 733	733MHz	133MHz	068Ah	22.8W	80°
Pentium-III 733	733MHz	133MHz	0686h	19.1W	80°
Pentium-III 700	700MHz	100MHz	068Ah	21.9W	80°
Pentium-III 700	700MHz	100MHz	0686h	18.3W	80°
Pentium-III 667	667MHz	133MHz	0686h	17.5W	82°
Pentium-III 650	650MHz	100MHz	0686h	17.0W	82°
Pentium-III 600EB	600MHz	133MHz	0686h	15.8W	82°
Pentium-III 600E	600MHz	100MHz	0686h	15.8W	82°
Pentium-III 550E	550MHz	100MHz	0683h	14.5W	85°
Pentium-III 533EB	533MHz	133MHz	0683h	14.0W	85°
Pentium-III 500E	500MHz	100MHz	0683h	13.2W	85°

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A special method to reduce power consumption is to force the processor into the 'Throttle Mode'. This is achieved by actuating the 'Stop Clock' input of the CPU, and can be activated through the BIOS settings. A Throttle Mode of 50% e.g. means a duty cycle of 50% on the stop clock input. However, while saving considerable power consumption, the data throughput of the processor is also reduced. The table below shows the effect of several throttle mode settings on the processor temperature in a given system equipped with the CC5-RAVE. The CPU is a 850MHz Pentium-III processor, the airflow around the CC5 cards slot is about 16m^3/h, which is typical for EKF systems. While the testing procedure, the CPU is stressed to its maximum by running kpower.exe.

Ambient Temperature °C Climate Chamber	Throttle Mode (PIII-850) °C							
	0% (100% duty)		25%		50%		87.5%	
	Board	Die	Board	Die	Board	Die	Board	Die
40	52	74	50	68	48	60	42	48
45	59	82	58	75	54	66	50	54
50	64	87	64	82	60	72	55	58
55	71	93	69	86	66	77	61	63
60	76	98	74	91	71	82	65	67
65	81	104	79	96	76	87	71	72
70	87	110	84	102	81	92	76	78
75	92	115	89	107	87	98	80	81
80	97	119	95	112	92	103	85	86
85	1)	1)	100	117	97	108	90	92
90			1)	1)	102	113	95	97
95					108	119	101	102
100					1)	1)	106	107

1) System not operational anymore

From the table on the previous page the maximum allowed die temperature of the PIII-850 can be derived as 80°C. If a small amount of overtemperature would be tolerated, the test system can be operated up to 45°C ambient temperature at 0% throttle mode, and up to 75°C at 87.5% throttle mode. However, the processor under test did remain fully functional up to ~120°C die temperature. Under typical conditions (not executing kpower.exe), the heat dissipation of the CPU would be remarkable lower, thus increasing the maximum ambient temperature of the CC5-RAVE.

The table below shows the effect of several throttle mode settings on the processor temperature in a given system equipped with the CC5-RAVE, now provided with a 566MHz Celeron processor. Again, the airflow around the CC5 cards slot is about 16m^3/h, which is typical for EKF systems, and as before, while the testing procedure, the CPU is stressed to its maximum by running kpower.exe.

Ambient Temperature °C Climate Chamber	Throttle Mode (Celeron-566) °C							
	0% (100% duty)		25%		50%		87.5%	
	Board	Die	Board	Die	Board	Die	Board	Die
40	48	66	48	62	46	56	42	43
45	56	74	54	69	51	61	48	49
50	61	80	59	74	57	67	52	53
55	66	85	64	78	62	72	58	59
60	71	90	69	83	67	77	63	64
65	76	97	74	88	72	82	68	69
70	82	104	81	97	77	87	72	74
75	88	109	86	101	82	92	78	80
80	94	117	92	109	87	98	84	85
85	98	121	96	115	93	104	88	90
90	1)	1)	103	121	98	110	94	95
95			1)	1)	103	115	99	99
100					108	121	104	106

1) System not operational anymore

The maximum allowed die temperature of the Celeron-566 can be derived as 90°C. The test system can be operated up to 60°C ambient temperature at 0% throttle mode (which is 100% duty cycle), and up to 85°C at 87.5% throttle mode. However, the processor under test did remain fully functional up to ~120°C die temperature. Under typical conditions (not executing kpower.exe), the heat dissipation of the CPU would be remarkable lower, thus increasing the maximum ambient temperature of the CC5-RAVE.

The measuring results in the table above are based on a forced vertical airflow of 16m^3/h around each card slot in a fully equipped 19-inch system rack, achieved by three Papst 4312M fans operated at 12V. Under these conditions, the CC5 heatsink delivers a thermal resistance of about 1K/W.

What can be recommended as an optimum airflow? The table below shows the effect on the maximum allowable ambient temperature of our PIII-850 system at the specified maximum processor die temperature of 80°C. Again, the processor is stressed to its maximum power dissipation by running kpower.exe.

Fan Type Pabst x 3	Vertical Airflow around each Card Slot	Maximum Ambient Temp. @Throttle Mode			
		0%	25%	50%	87.5%
4312GL/6V	4m^3/h	20°C	35°C	44°C	69°C
4312GL/12V	10m^3/h	31°C	43°C	55°C	73°C
4312M/12V	16m^3/h	42°C	48°C	57°C	74°C
4312-179/13.2V	27m^3/h	43°C	50°C	60°C	75°C

As easily can be seen, increasing the airflow above 16m^3/h has no significant effect on the maximum allowable ambient temperature. So ~16m^3/h would be the optimum airflow for most industrial systems.

<u>Conclusion</u>
Take care of sufficient heat exchange in your system. If appropriate, setup the Throttle Mode feature. Both Celeron and Pentium-III processors can be reliably operated over a wide temperature range in a suitable environment.

Main Memory

The CC5-RAVE is equipped with a socket for installing a single 144-pin SO-DIMM module (module height limited to <=1.100 inch). Minimum memory size is 32MB; maximum memory size is 256MB. Due to the video requirements of the i810 chipset, minimum memory for the Windows NT 4.0 and Windows 2000 operating system is 64MB (some of the system memory is dedicated to the graphics controller). The supported on-board memory is entirely chacheable. The memory module is a unbuffered SD-RAM, PC100 style. The contents of the SPD eeprom are displayed on system start by the BIOS. The memory clock is 100MHz maximum, due to limitations of the 810GMCH.

LAN Subsystem

The Intel 82559ER Fast Ethernet PCI LAN subsystem provides both 10Base-T and 100Base-TX connectivity. Features include:

- PCI bus mastering 32-bit, 33MHz
- Shared memory structure in the host memory that copies data directly to/from host memory
- 10Base-T (Ethernet) and 100Base-TX (Fast Ethernet, half- or full-duplex) capability using a single RJ-45 connector
- IEEE 802.3µ Auto-Negotiation for the fastest available connection
- Jumperless configuration (complete software-configurable)

Two display LEDs in the RJ-45 connector signal LAN Link and Activity status.

The Intel 82559ER Fast Ethernet PCI LAN software and drivers are available from Intel's World Wide Web site.

Enhanced IDE Interface

The EIDE interface handles the exchange of information between the processor and peripheral devices like hard disks, ATA CompactFlash cards and CD-ROM drives. The interface supports:

- Up to three ATA devices (2 IDE, 1 CompactFlash)
- PIO Mode 3/4, Ultra ATA/33, Ultra ATA/66
- Support for LS-120 drives

The primary IDE interface is routed to a standard 40-pin header, allowing master and slave device attached to one common flat ribbon cable (use special 80-pin cabling assembly for Ultra ATA/66 operation).

The presence of a 80-pin cable at the primary IDE interface could be checked out by reading the state of the GPI0 of the Firmware Hub (FWH). The ATA standard defines the signal PDIAG-/CBLID- for identifying the cable. This line is routed to GPI0 of the FWH. A logical 1 signals a 40-pin, a logical 0 a 80-pin cable. See the ATA/ATAPI-6 specification (section 6.7 “Host determination of cable type by detecting CBLID-“) for details.

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The secondary IDE interface is routed to the CompactFlash Card Adapter socket. Use this connector to attach a CompactFlash ATA style silicon disk, whenever a hard disk is not suitable for your system, or as an additional mass storage device.

A display LED, situated in the front panel near the reset push-button, signals disk activity status of the primary IDE devices and also the CompactFlash slot. This LED is also software programmable. See the section “Programmable LED” how to do this.

Graphics Subsystem

The graphics subsystem is part of the Intel 82810 Graphic/Memory Controller Hub (GMCH), supporting the following features:

- 3-D Hyper Pipelined architecture
- Full 2-D hardware acceleration
- Motion video acceleration
- 3-D graphics visual and texturing enhancements
- Integrated 24-bit 230MHz RAMDAC
- DDC2B compliant
- Hardware motion compensation for software MPEG2 decode
- Integrated graphics memory controller

The CC5-RAVE is provided with the DVI-I graphics connector. This is both a digital and analog interface. Recent digital input flat-panel displays are already available with this connector style. Adapter cables can be used for converting to the 15-pin HD-SUB connector.

A special display transmitter chip is used for serializing/deserializing the differential DVI signals. The SiI 154 (Silicon Image) transmitter uses PanelLink® Digital technology to support displays ranging from VGA to SXGA resolutions (25 - 112Mpps) in a single link interface. The SiI 154 transmitter has a highly flexible interface with 12-bit (½ pixel) or 24-bit 1 pixel/clock input for true color (16.7 million) support. It can be foreseen, that DVI will overcome the legacy analog and proprietary digital interfaces in the near future.

i810 GMCH Refresh Rates						
Resolution	Color	60Hz	70Hz	72Hz	75Hz	85Hz
640x200	16		!			
640x350	16		!			
640x400	256	!	!		!	!
	64K	!	!		!	!
	16M		!			
640x480	16	!		!	!	!
	256	!	!	!	!	!
	32K	!			!	!
	64K	!	!	!	!	!
	16M	!	!	!	!	!
800x600	256	!	!	!	!	!
	32K	!			!	!
	64K	!	!	!	!	!
	16M	!	!	!	!	!
1024x768	256	!	!		!	!
	32K	!			!	!
	64K	!	!	!	!	!
	16M	!	!	!	!	!
1056x800	16		!			
1280x1024	256	!	!	!	!	!
	32K	!			!	!
	64K	!	!	!	!	!
	16M	!	!	!	!	!

Real-Time Clock

The CC5-RAVE has a time-of-day clock and 100-year calendar. A battery on the board keeps the clock current when the computer is turned off. The CC5 uses a Vanadium-Pentoxide-Lithium rechargeable battery, giving an autonomy of more than 80 days when fully loaded after 24 hours. The cell is free of memory effects and withstands deep discharging. Under normal conditions, replacement should be superfluous during lifetime of the board.

Universal Serial Bus (USB)

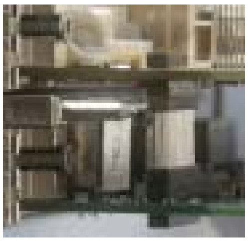
The CS5-RAVE is provided with a single USB port, routed to a front panel connector. You can connect a USB peripheral device directly to the CC5 without an external hub. To attach more devices, connect an external hub to the CC5 built-in port (often monitors or keyboards provide USB hub functionality). The USB connector can source up to 0.5A/5V, and is protected by a Polyswitch resettable fuse against shortening.

LPC Super- I/O Interface

In a modern system, legacy ports as PS/2 Keyboard/Mouse, COM1/2 and LPT have been replaced by USB and Ethernet connectivity. The 1.4MB floppy disk drive has been swapped against LS-120 or CD-RW drives, attached to the IDE connector. Hence, the CC5-RAVE is virtually provided with all necessary I/O ports.

Though, for applications with inevitable demand for legacy I/O, EKF offers the CC6-ACID, an expansion module to the CC5-RAVE, featuring all classic Super-I/O functionality. The CC6-ACID is a 3U Eurocard, with an either 8HP (double) or 4HP (single) width front panel. Access to the connectors COM1/2, LPT, mouse, keyboard is given directly from the front panel. Onboard connectors are provided for FDD, MIDI/Gameport, and cooling fans. Optionally, the CC6 is available with an onboard 2.5" hard disk drive. The CC6-ACID connects to the CC5-RAVE across the connector LPCT or LPCB (LPC = Low Pin Count interface standard). The CC6-ACID can be attached either to the top of the CC5-RAVE or to the bottom (bottom attachment restricted to the 4HP version of the CC6-ACID).

The photo above (left) shows the bottom attachment of the CC6-ACID. The boards are fixed together by the LPC connector and the IDE connector, and in addition by a bracket which bolts together both front panels. The right image shows the top attachment of the CC6-ACID.



The photo above (left) shows the CC5-RAVE and CC6-ACID connected by the LPC interface. The right image shows the front panel fixing bracket.

Together, the CC5-RAVE and the CC6-ACID represent an ultra-compact, complete desktop functionality, industrial grade computer system.

Watchdog/Reset

The CC5-RAVE is provided with the MAX705 supervisor circuit, which controls the supply voltages 3.3V, 5V and the CPU core voltage, and generates a power-on reset signal. The manual push-button reset is also passed through the MAX705 for appropriate pulse conditioning.

The reset manual push-button is situated at the front panel. The button is indent mounted behind the front and requires a tool, e.g. pen to be pressed, preventing from being inadvertently activated. The push button reset signal is routed across a PLD (programmable logic device) and could be passivated on customers request.

The healthy state of the CC5-RAVE is signalled by the LED PWR integrated into the reset push-button. As soon as this LED begins to shine all power voltages are well and the reset signal was deasserted.

Another feature is the watchdog function, which can be be programmed by software. The behaviour of the MAX705 watchdog is partially defined by the PLD, which controls whether the watchdog is activated. The related software (e.g. BIOS, application program) must trigger the watchdog by toggling the GPIO21 signal of the ICH 82801.

The watchdog is in a passive state after a system reset. There is no need to trigger it at boot time. Once the GPIO21 of the ICH was pulsed the watchdog is activated. If the duration between two trigger pulses exceeds a period of 1000 ms the watchdog timed out and a system reset is generated.

The watchdog remains in the active state until the next system reset. There is no way to disable it once it was started.

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Firmware Hub (Flash BIOS)

The BIOS is stored in the 82802Ax Firmware Hub (there are second sources available with deviant part numbers). The firmware hub contains a nonvolatile memory core based on flash technology, allowing the BIOS to be upgraded. Currently, there are three variants of the FWH available:

x = A: 2Mbit
x = B: 4Mbit
x = C: 8Mbit

The FWH is soldered at the bottom side of the CC5-RAVE. In addition to storing the system BIOS, the firmware hub incorporates logic features such as hardware random number generator (RNG).

The latest CC5-RAVE BIOS is available from the EKF website.

Programmable LED

The CC5-RAVE offers a software programmable LED, marked as IDE (placed near the reset push-button). After system reset, this LED defaults to signal the IDE activity. By the first setting of the GPIO22 of the ICH 82801 this LED changes its function and is then controlled only by the level of the GPIO22 pin. Setting this pin to 1 will switch on the LED.

The LED IDE remains in the programmable state until the next system reset.

Hot Swap Detection

The CompactPCI specification added the signal ENUM# to the PCI bus to allow the system hot swapping. This signal is routed to the GPIO8 of the ICH 82801 on the CC5-RAVE. A System Management Interrupt (SMI) can be requested if ENUM# changes by insertion or removal of a board.

Note that the CC5-RAVE itself isn't a hot swap device, because it makes no sense to remove the system controller from a CompactPCI system. However, it is capable to recognize the hot swap of peripheral boards and to start software that is doing any necessary system reconfiguration.

Power Supply Status (DEG#, FAL#)

Power supply failures may be detected before the system crashs down by monitoring the signals DEG# or FAL#. These low active lines are additions of the CompactPCI specification and may be driven by the power supply.

DEG# signals the degrading of the supply voltages, FAL# there possible failure.

On the CC5-RAVE FAL# is routed to the GPIO12 and DEG# to the GPIO13 of the ICH 82801.

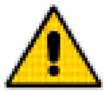
PXI Trigger Signals

The CC5-RAVE supports two trigger signals of the PXI standard defined by National Instruments. Trigger line 0 is routed to the GPIO9 and line 7 to the GPIO10 of the ICH 82801.

Installing and Replacing Components

Before You Begin

Warnings



The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect the system from its power source and from any telecommunication links, networks or modems before performing any of the procedures described in this chapter. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage. Some parts of the system can continue to operate even though the power switch is in its off state.

Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis or board front panel. Store the board only in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for rapair.

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Installing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system

- Remove the board packaging, be sure to touch the board only at the front panel
- Identify the related CompactPCI slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return

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Removing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system

- Identify the board, be sure to touch the board only at the front panel
- unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only

Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.

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EMC Recommendations

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

Reccomended Accessories

Blind CPCI Front Panels	EKF Elektronik	Widths currently available (1HP=5.08mm): with handle 4HP/8HP without handle 2HP/4HP/8HP/10HP/12HP
Ferrit Bead Filters	ARP Datacom, 63115 Dietzenbach	Ordering No. 102 820 (cable diameter 6.5mm) 102 821 (cable diameter 10.0mm) 102 822 (cable diameter 13.0mm)
Metal Shielding Caps	Conec-Polytronic, 59557 Lippstadt	Ordering No. CDFA 09 165 X 13129 X (DB9) CDSFA 15 165 X 12979 X (DB15) CDSFA 25 165 X 12989 X (DB25)

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Installing or Replacing the Processor

Note: If you decide to install a processor on your own, observe the precautions in 'Before You Begin'

As default, the CC5-RAVE comes fully equipped and tested with a processor. So normally there should be no need to install a processor.

Due to the very compact construction of the CC5-RAVE, a ZIF socket for the processor could not implemented. Instead, the CC5 features a high quality industrial PGA 370 socket with precision contacts. You will need a special tool to remove the processor from this socket. If you try to remove the CPU without the PGA extracting tool, the processors case or its contact pins could be damaged. We suggest that you install or replace the processor only if you own an ESD workstation and the matching extracting tool.

Before the processor can be replaced, you would have to remove the passive heatsink, which is fitted by screws to the board and attached by conductive pads and/or adhesion to the processor. Special handling is required to remove the heatsink and to re-install it afterwards, including renewing the conductive adhesion and adjustment of the mounting screws.

Conclusion: Do not attempt to replace the processor by yourself, unless you are an absolute professional. Instead, send in the board to EKF.

Installing or Replacing the Memory Module

Note: If you decide to replace the memory, observe the precautions in 'Before You Begin'

By default, the CC5-RAVE comes fully equipped and tested with a 64MB...256MB SD-RAM memory module. So normally there should be no need to install a memory module.

Because the main memory is also used as video memory, the CC5-RAVE requires a PC-100 (100MHz) SDRAM SO-DIMM module even when the processor front side bus is 66MHz (Celeron only). It is highly recommended that Serial Presence Detect (SPD) SO-DIMMs be used, since this allows the chipset to accurately configure the memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted.

A replacement memory module must match the 144-pin SO-DIMM form factor (known from Notebook PCs), 3.3V, 100MHz unbuffered, non-ECC style. Be sure to buy no module with a height >1.100 inch. Suitable modules are available up to 256MB. The 810GMCH supports modules of up to a maximum of 12 address lines (A0...A11). However, there are also 256MB memory modules on the market organized by 13 address lines, which are not suitable.

Conclusion: Replacement of a memory module is easy, but unnecessary in most cases.

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Replacement of the Battery

When your system is turned off, a battery maintains the current time-of-day clock and the values in CMOS RAM current. The battery is rechargeable und should last during the lifetime of the CC5-RAVE. For replacement, the old battery must be desoldered, and the new one soldered. Observe the cell polarization. We suggest that you send back the board to EKF for battery replacement.

Warning

Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type. Do not expose a battery to fire.

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Technical Reference

Local PCI Devices

The following table shows the on-board PCI devices and their location within the PCI configuration space. These devices consist of the Ethernet controller, the PCI-To-PCI Bridge and several devices within the i810 chip set.

Bus Number	Device Number	Function Number	Vendor ID	Device ID	Description
0	0x00	0	0x8086	0x7120 [1])	Host Bridge
0	0x01	0	0x8086	0x7121 [2])	VGA Display
0	0x1E	0	0x8086	0x2418	PCI-To-PCI Bridge
0	0x1F	0	0x8086	0x2410	ISA Bridge
0	0x1F	1	0x8086	0x2411	IDE Controller
0	0x1F	2	0x8086	0x2412	USB Controller
0	0x1F	3	0x8086	0x2413	SMB Controller
1	0x04	0	0x8086	0x1209	Ethernet Controller
1	0x06	0	0x104C	0xAC28	PCI-To-PCI Bridge (CPCI)

[1]) 0x7122 when i810E chip set is equipped.
[2]) 0x7123 when i810E chip set is equipped.

Local SMB Devices

The CC5-RAVE contains a few devices that are reachable via the System Management Bus (SMB). These are the clock generation chip, the SPD EEPROM on the SO-DIMM memory module and a CPU temperature controlling device in particular. Other devices could be connected to the SMB via the *CompactPCI* signals IPMB SCL (J1 B17) and IPMB SDA (J1 C17).

Address	Description
0x30	CPU Temperature Sensor MAX 1617
0xA0	SPD of SO-DIMM
0xD2	Main Clock Generation ICS 9250-16

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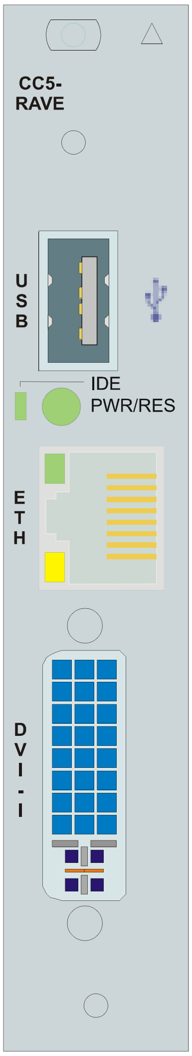
Connectors

Caution

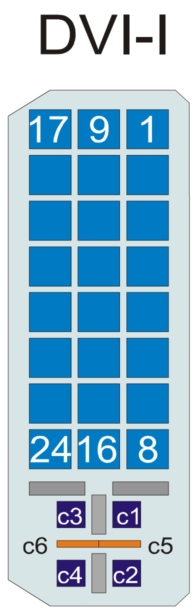
Some of the internal connectors provide operating voltage (e.g. 5V and 12V) to devices inside the system chassis, such as fans and internal peripherals. Not all of these connectors are overcurrent protected. Do not use these internal connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.



CC5-RAVE Front Panel Elements

Video Monitor Connector DVI-I

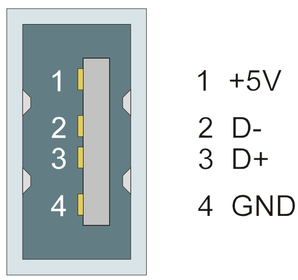
DVI-I					
17	tx0-	9	tx1-	1	tx2-
18	tx0+	10	tx1+	2	tx2+
19	GND	11	GND	3	GND
20		12		4	
21		13		5	
22	GND	14	ddcpow	6	ddcl
23	txc+	15	GND	7	ddca
24	txc-	16	dvihp	8	vsync
	c3	blue	c1	red	
	c6	GND	c5	GND	
	c4	hsync	c2	green	



For attachment of an ordinary analog RGB monitor to the DVI receptacle, there are both adapters and also adapter cables available to the HD-SUB15 connector. Attachment of digital monitors (flat panel displays) should be done by means of a DVI to DVI cable (single link style cable is sufficient).

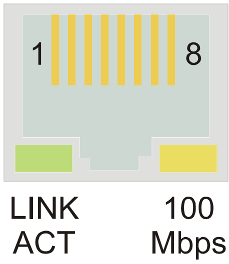
USB Connector

1	+5V (PolySwitch 0.75A)
2	USB Data 0 (1) NEG
3	USB Data 0 (1) POS
4	GND



Ethernet Connector

RJ45	
1	TX+
2	TX-
3	RX+
4	
5	
6	RX-
7	
8	



The yellow LED signals 100Mbit/s when lit, and 10Mbit/s when off. The green LED indicates LINK established when continuously on, and data transfer (activity) when blinking. If the green LED is off, no LINK is established.

LPC Low Pin Count Header

PLPCT/PLPCB			
GND	1	2	pciclk
GND	3	4	lad0
GND	5	6	lad1
GND	7	8	lad2
GND	9	10	lad3
GND	11	12	lframe#
GND	13	14	ldrq#
serirq	15	16	lpme#
lsmi#	17	18	pcirst#
5V	19	20	3.3V
rcin#	21	22	a20gate
12V	23	24	3.3V
sio_clk14	25	26	speaker

The LPC header is available twice, on both sides of the board, top and bottom, in order to provide attachment of the CC6-ACID either to the left or to the right side of the CC5-RAVE.

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ATA/IDE Header

PIDE			
reset#	1	2	GND
pd07	3	4	pd08
pd06	5	6	pd09
pd05	7	8	pd10
pd04	9	10	pd11
pd03	11	12	pd12
pd02	13	14	pd13
pd01	15	16	pd14
pd00	17	18	pd15
GND	19	20	KEY
pdmarq	21	22	GND
piow#	23	24	GND
pior#	25	26	GND
piordy	27	28	470 Ohm PD
pdmack#	29	30	GND
intrq (IRQ 14)	31	32	
pda1	33	34	p66detect
pda0	35	36	pda2
pcs0#	37	38	pcs1#
pideact#	39	40	GND

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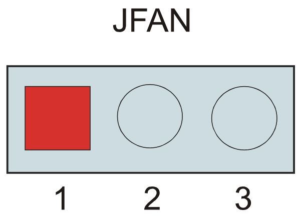
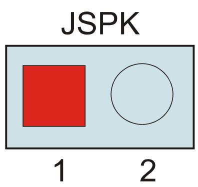
Fan Heatsink Header



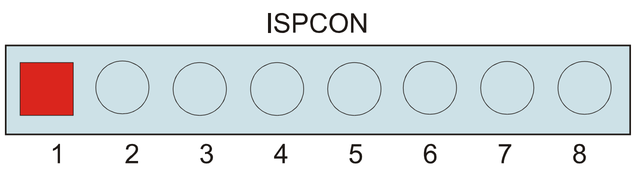
1 +5V
2 GND
3 +12V

Speaker Header



1 +5V
2 Speaker

PLD Programming Header



1 +5V
2 serial data out
3 serial data in
4 ispGAL enable
5 NC
6 mode
7 GND
8 serial clock

Note: The ISPCON is not normally stuffed. Its footprint is situated at the bottom side of the board.

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Processor Debug Header

PITP			
itpres#	1	2	GND
dbreset#	3	4	GND
tck	5	6	GND
tms	7	8	tdi
itppon	9	10	tdo
	11	12	trst#
GND	13	14	
GND	15	16	itpreq#
GND	17	18	itprdy#
GND	19	20	
GND	21	22	
GND	23	24	
GND	25	26	
GND	27	28	
itpclk	29	30	

Note: The Debug Header is not normally stuffed. Its footprint is situated at the bottom side of the board.

CompactPCI J1

#J1	A	B	C	D	E
25	5V	*REQ64#*	ENUM#	3.3V	5V
24	AD1	5V	VI/O	AD0	*ACK64#*
23	3.3V	AD4	AD3	5V	AD2
22	AD7	GND	3.3V	AD6	AD5
21	3.3V	AD9	AD8	M66EN (GND)	C/BE0#
20	AD12	GND	VI/O	AD11	AD10
19	3.3V	AD15	AD14	GND	AD13
18	SERR#	GND	3.3V	PAR	C/BE1#
17	3.3V	IPMB SCL	IPMB SDA	GND	PERR#
16	DEVSEL#	GND	VI/O	STOP#	LOCK#
15	3.3V	FRAME#	IRDY#	GND	TRDY#
14					
13					
12					
11	AD18	AD17	AD16	GND	C/BE2#
10	AD21	GND	3.3V	AD20	AD19
9	C/BE3#	IDSEL	AD23	GND	AD22
8	AD26	GND	VI/O	AD25	AD24
7	AD30	AD29	AD28	GND	AD27
6	REQ#	GND	3.3V	CLK	AD31
5	*BRSVP1A5*	*BRSVP1B5*	RST#	GND	GNT#
4	IPMB PWR	GND	VI/O	INTP	*INTS*
3	INTA#	INTB#	INTC#	5V	INTD#
2	*TCK*	5V	*TMS*	*TDO*	*TDI*
1	5V	-12V	*TRST#*	+12V	5V

pin positions printed italic/coloured brown: not connected
pin positions printed italic/coloured blue: not connected
pin positions printed italic/coloured gray: pull up 1k to Vio

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CompactPCI J2

#J2	A	B	C	D	E
22	*GA4*	*GA3*	*GA2*	*GA1*	*GA0*
21	CLK6	GND	*RSV*	*RSV*	*RSV*
20	CLK5	GND	*RSV*	GND	*RSV*
19	GND	GND	*RSV*	*RSV*	*RSV*
18	*BRSVP2A18*	*BRSVP2B18*	*BRSVP2C18*	GND	*BRSVP2E18*
17	*BRSVP2A17*	GND	PRST#	REQ6#	GNT6#
16	*BRSVP2A16*	PXI TRIG0	DEG#	GND	PXI TRIG7
15	*BRSVP2A15*	GND	FAL#	REQ5#	GNT5#
14	*AD35*	*AD34*	*AD33*	GND	*AD32*
13	*AD38*	GND	V(I/O)	*AD37*	*AD36*
12	*AD42*	*AD41*	*AD40*	GND	*AD39*
11	*AD45*	GND	V(I/O)	*AD44*	*AD43*
10	*AD49*	*AD48*	*AD47*	GND	*AD46*
9	*AD52*	GND	V(I/O)	*AD51*	*AD50*
8	*AD56*	*AD55*	*AD54*	GND	*AD53*
7	*AD59*	GND	V(I/O)	*AD58*	*AD57*
6	*AD63*	*AD62*	*AD61*	GND	*AD60*
5	*C/BE5#*	GND (64EN#)	V(I/O)	*C/BE4#*	*PAR64*
4	V(I/O)	*BRSVP2B4*	*C/BE7#*	GND	*C/BE6#*
3	CLK4	GND	GNT3#	REQ4#	GNT4#
2	CLK2	CLK3	SYSEN#	GNT2#	REQ3#
1	CLK1	GND	REQ1#	GNT1#	REQ2#

pin positions printed italic/coloured gray: 1k to Vio
pin positions printed italic/coloured brown: not connected

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Power Supply Requirements

Operating Voltage	max. current (depends on CPU in use)
+5V / ±0,25V	7.0A
+3,3V / ±0,1V	3.5A
+12V / ±0,5V	0.5A
-12V / ±0,5V	-

Literature

Theme	Document Title	Origin
CompactPCI Specification	*CompactPCI* Specification, PICMG 2.0 R3.0, Oct. 1, 1999	PICMG (http://www.picmg.org)
USB Specification	Universal Serial Bus Specification	http://www.teleport.com/~usb
PCI	PCI Hardware and Software Architecture & Design, Solari/Willse, 4th Edition, Annabooks	Annabooks (http://www.annabooks.com)
Metric Connectors	IEC 1076-4-101 Application Literature from ERNI, AMP, FCI	Beuth Verlag, Berlin ILI Index House, GB SL57EU Ascot Berkshire
2.54mm Shrouded Headers	DIN 41651	Beuth Verlag, Berlin

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